order data elements from the first and the second pluralities of packed data elements, the opcode field specifying data elements selected from the group consisting of byte elements, word elements and doubleword elements.

38. The apparatus of Claim 37 wherein the opcode field of the unpack instruction contains one of a set of operation codes comprising the hexadecimal values 0F68, 0F69 and 0F6A.

REMARKS

The foregoing amendment is provided to impart precision to the claims and to place them in condition for allowance, by more particularly pointing out the invention, rather than to avoid prior art.

Applicants respectfully request reconsideration of this application as amended. Claims 15-38 are pending. Claims 19-23 are restricted and withdrawn from consideration. Claims 16-18 are allowed. Claims 15-18, 24-28, 31-33, 35 and 37 are amended. Claim 34 is cancelled.

The remaining comments are directed to Claim 15 and Claims 24-38. The Office Action mailed on December 21, 2001 rejects Claim 15 under the judicially created doctrine of obvious-type double patenting as being unpatentable over Claim 2 of U.S. Patent No. 5,802,336.

A terminal disclaimer in compliance with 37 CFR 1.321(c) is submitted herewith. Accordingly, Applicant respectfully requests the Examiner withdraw his rejection of Claim 15, for nonstatutory double patenting.

The Office Action rejects Claims 24-38 under 35 U.S.C. 112, second paragraph, as being indefinite. The Examiner states that language in Claim 24 is inconsistent with the limitations of Claim 15. Applicant respectfully disagrees, but has amended Claims 15

and 24 to more particularly point out the invention and place them in condition for allowance. Applicant respectfully requests reconsideration of Claims 24-33, as amended.

The Examiner also states that language in Claim 34 is inconsistent with the limitations of Claim 15. Claim 34 is cancelled herewith, and Claims 35 and 37 have been amended to depend from Claim 15 and place them in condition for allowance. Applicant, therefore respectfully requests reconsideration of Claims 35-38, as amended.

Applicants believe that Claims 15-18, Claims 24-33 and Claims 35-38 are presently in condition for allowance and such action is earnestly solicited.

CONCLUSION

Applicants respectfully submit the present claims for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call John Ward at (408) 720-8300, x237.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: February 21, 2002

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE ABSTRACT:

Please replace the abstract on page 41 of the present application, with the amended abstract on the separate sheet attached.

IN THE SPECIFICATION

At Page 1, line 3, please insert:

RELATED APPLICATIONS

Continuation of application Ser. No. 08/974,435, filed Nov. 20, 1997, now Pat. No. 6,119,216, which is a Divisional of Ser. No. 08/791,003, filed Jan. 27, 1997, now Pat. No. 5,802,336, which is a Continuation of Ser. No. 08/349,047, filed Dec. 2, 1994, abandoned.

At page 21, line 6 please replace "_____, serial number _____" with -- Dec. 21, 1994, serial number 349,040, now abandoned--.

At page 21, lines 7-8 please replace "_____, serial number _____" with -- Dec. 1, 1994, serial number 349,559, now abandoned--.

At page 21, lines 8-9 please replace "_____, serial number _____" with -- Dec. 1, 1994, serial number 349,730, now abandoned --.

At page 21, line 10 please insert--now abandoned,-- after "08/176,123,".

At page 21, line 12 please insert--now abandoned,-- after "08/175,772,".

IN THE CLAIMS:

Claims 15-18, 24-28, 31-33, 35 and 37 are amended.

Claim 34 is cancelled.

15. (Amended Once) An apparatus comprising:

a instruction decoder to receive an unpack instruction;

a first source register to hold a first packed data having a first plurality of packed data elements including a first packed data element and a third packed data element;

a second source register to hold a second packed data having a second plurality of packed data elements including a second packed data element and a fourth packed data element;

a [third] destination register to hold a third packed data;

a circuit coupled to the decoder to receive the first packed data from the first source register and the second packed data from the second source register and to unpack the first packed data and the second packed data responsive to the unpack instruction[s] by copying the first packed data element into the [third] destination register, copying the second packed data element into the [third] destination register adjacent to the first packed data element, copying the third packed data element into the [third] destination register adjacent to the second packed data element, and copying the fourth packed data element into the [third] destination register adjacent to the third packed data element.

16. (Amended Once) A digital processing apparatus comprising:

a decoder to receive an unpack control signal having an Intel integer opcode format comprising three or more bytes, a third byte of the three or more bytes permitting a first three-bit source register address and a second three-bit source-destination register address;

a first register to hold a first packed data having a first plurality of packed data elements including a first packed data element and a third packed data element, the first register corresponding to the first three-bit source register address;

a second register to hold a second packed data having a second plurality of packed data elements including a second packed data element and a fourth packed data element, the second register corresponding to the second three-bit source-destination register address;

a circuit to receive the first packed data from the first register and the second packed data from the second register, and in response to the unpack control signal, to copy the first packed data element into the second register, copy the second packed data element into the second register adjacent to the first packed data element, copy the third packed data element into the second register adjacent to the second packed data element, and copy the fourth packed data element into the second register adjacent to the third packed data element.

17. (Amended Once) The digital processing apparatus recited in Claim 16 wherein the decoder is further to receive the unpack control signal having an Intel integer opcode format as described in the "Pentium® Processor Family User's Manual," the Intel integer opcode format comprising three or more bytes, a first byte and a second byte of the three or more bytes permitting an operation code to specify an unpack operation interleaving low order packed byte elements, word elements or doubleword elements from the first and second packed data;

18. (Amended Once) A computer system comprising:

a memory to hold an unpack instruction having an Intel integer opcode format comprising three or more bytes, one of the three or more bytes permitting a first three-bit source register address and a second three-bit source-destination register address;

a storage device to hold software, the software configured to supply the unpack instruction to the memory for execution;

a processor enabled to receive and decode the unpack instruction from the memory, the processor including: a first register corresponding to the first three-bit source register address to hold a first packed data having a first plurality of packed data elements including a first packed data element and a third packed data element, a second register corresponding to the second three-bit source-destination register address to hold a second packed data having a second plurality of packed data elements including a second packed data element and a fourth packed data element, and a circuit to receive the first packed data from the first register and the second packed data from the second register and to copy the first packed data element into the second register, copy the second packed data element into the second register adjacent to the first packed data element, copy the third packed data element into the second register adjacent to the second packed data element, and copy the fourth packed data element into the second register adjacent to the third packed data element.

19. A method comprising:

receiving an unpack instruction, said unpack instruction comprising an opcode field, a first field to indicate a first operand having a first plurality of data elements including a first data element and a second data element, and a second field to indicate a second operand having a second plurality of data elements including a third data element and a fourth data element, each of the first data element, the second data element, the third data element, and the fourth data element having a length of N/2 bits;

storing an unpacked data element having a length of N bits in response to said unpack instruction, said unpacked data element comprising the first data element but not the second data element of the first operand, and the third data element but not the fourth data element of the second operand.

20. The method recited in Claim 19 wherein the first data element is a low order data element of the first operand and the third data element is a low order data element of the second operand and the opcode field of the unpack instruction contains one of a set of operation codes to specify an unpack operation interleaving low order byte elements, word elements or doubleword elements from the first and the second pluralities of data elements.

21. The method recited in Claim 20 wherein the opcode field of the unpack instruction contains one of a set of operation codes comprising the hexadecimal values 0F60, 0F61 and 0F62.

22. The method recited in Claim 20 wherein the first data element is a high order data element of the first operand and the third data element is a high order data element of the second operand and the opcode field of the unpack instruction contains one of a set of operation codes to specify an unpack operation interleaving high order byte elements, word elements or doubleword elements from the first and the second pluralities of data elements.

23. The method recited in Claim 22 wherein the opcode field of the unpack instruction contains one of a set of operation codes comprising the hexadecimal values 0F68, 0F69 and 0F6A.

24. (Amended Once) The apparatus of Claim 15, the unpack instruction having an Intel integer opcode format comprising three bytes, a third byte of the three bytes permitting a [first] source register address and a [second] source-destination register address.

25. (Amended Once) The apparatus of Claim 24, the [first] source register address and the [second] source-destination register address each consisting of three bits.

26. (Amended Once) The apparatus of Claim 24, the first source register corresponding to the [first] source register address.

27. (Amended Once) The apparatus of Claim 24, the second source register corresponding to the [second] source-destination register address.

28. (Amended Once) The apparatus of Claim 27, the [third] destination register corresponding to the [second] source-destination register address.

29. The apparatus of Claim 24 wherein the decoder further decodes the unpack instruction, a first byte and a second byte of the three bytes comprising an operation code specifying an unpack operation to interleave low order packed elements from the first and second packed data, the elements selected from the group consisting of byte elements, word elements and doubleword elements.

30. The apparatus of Claim 24 further comprising:

a memory to hold the unpack instruction; and

a storage device to hold software, the software configured to supply the unpack instruction to the memory for execution.

31. (Amended Once) The apparatus of Claim 30, the instruction decoder to receive and decode the unpack instruction from the memory, the first source register corresponding to

the [first] source register address, the second source register corresponding to the [second] source-destination register address.

32. (Amended Once) The apparatus of Claim 31, the [third] destination register corresponding to the [second] source-destination register address.

33. (Amended Once) The apparatus of Claim 32, the [first] source register address and the [second] source-destination register address each consisting of three bits.

34. (Cancelled) The apparatus of Claim 15 wherein each of the first packed data element, the second packed data element, the third packed data element, and the fourth packed data element has a length of N/2 bits; and the circuit is coupled to the decoder to unpack the first packed data and the second packed data to produce an unpacked data element having a length of N bits in response to the unpack instruction, said unpacked data element comprising the first packed data element but not the third packed data element of the first packed data, and the second packed data element but not the fourth packed data element of the second packed data.

35. (Amended Once) The apparatus of Claim [34] 15 wherein the first packed data element is a low order data element of the first packed data and the second packed data element is a low order data element of the second packed data and the unpack instruction comprises an opcode field to contain one of a set of operation codes to specify an unpack operation interleaving low order data elements from the first and the second pluralities of packed data elements, the opcode field specifying data elements selected from the group consisting of byte elements, word elements and doubleword elements.

36. The apparatus of Claim 35 wherein the opcode field of the unpack instruction contains one of a set of operation codes comprising the hexadecimal values 0F60, 0F61 and 0F62.

37. (Amended Once) The apparatus of Claim [34] 15 wherein the first packed data element is a high order data element of the first packed data and the second packed data element is a high order data element of the second packed data and the unpack instruction comprises an opcode field to contain one of a set of operation codes to specify an unpack operation interleaving high order data elements from the first and the second pluralities of packed data elements, the opcode field specifying data elements selected from the group consisting of byte elements, word elements and doubleword elements.

38. The apparatus of Claim 37 wherein the opcode field of the unpack instruction contains one of a set of operation codes comprising the hexadecimal values 0F68, 0F69 and 0F6A.